

C\$8221 NEW ENHANCED AT (NEAT™) DATA BOOK 82C211/82C212/82C215/82C206 (IPC) CHIPSet™

- 100% IBM™ PC/AT Compatible New Enhanced CHIPSet™ for 12MHz to 16MHz systems
- Supports 16MHz 80286 operation with only 0.5-0.7 wait states for 100ns DRAMs and 12 MHz operation with 150ns DRAMs, 0 wait state 12MHz operation with 80ns DRAMs
- Separate CPU and AT Bus clocks
- Page Interleaved Memory supports single bank page mode, 2 way and 4 way page interleaved mode
- Integrated Lotus-Intel-Microsoft Expanded Memory Specification (LIM EMS) Memory Controller. Supports EMS 4.0.

The CS8221 PC/AT compatible NEAT CHIPSet™ is an enhanced, high performance 4 chip VLSI implementation (including the 82C206 IPC) of the control logic used on the IBM™ Personal Computer AT. The flexible

- Software Configurable Command Delays, Wait states and Memory Organization
- Optimized for OS/2 operation
- Shadow RAM for BIOS and video ROM to improve system performance
- Complete AT/286 system board requires only 28 logic components plus memory and processor
- Targeted at Desktop PC/ATs, Laptops and CMOS Industrial Control Applications
- Available as four CMOS 84-pin PLCC or 100-pin PFP components.

architecture of the NEAT CHIPSet* allows it to be used in any 80286 based system.

The CS 8221 NEAT CHIPSet™ provides a complete 286 PC/AT compatible system,

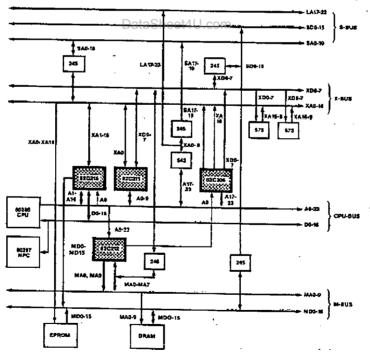


Figure 1. NEAT System Block Diagram

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